

Double Estimator

A New Receiver Principle for Tracking BOC Signals

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The United States and Europe have selected the binary offset carrier (BOC) modulation for navigation signals in the next-generation GNSS. However, BOC's multi-peaked correlation function is beginning to be recognized as creating a problem that still needs to be definitively solved: false lock or the tracking of secondary rather than the primary peak in the derived cross-correlation function. But now researchers have come up with a radically different approach of *two-dimensional correlation*, which combines two independent estimates of the input signal's time delay to create a single joint estimate that fully exploits the capabilities of BOC without running into problems of false lock.

For the current civilian GPS C/A code transmission with which people are most familiar, each GNSS satellite transmits an individual periodic code employing the principle of code division multiple access (CDMA). The code itself is modulated onto a carrier using a phase shift keying or PSK(f_c) technique where f_c is a code rate. The aim of signal processing design, then, is to estimate the relative delay in each incoming satellite signal, in order to compute the location of the receiver.

Time and technology move on. Based on a 2004 agreement between the European Union and the United States, the new European Galileo and the up-graded American GPS will make substantial use of the different modulation called Binary Offset Carrier (BOC).

Essentially, BOC multiplies a *subcarrier* as well as a code, onto the carrier. Standard nomenclature is BOC(f_s, f_c) where f_s is a subcarrier frequency and f_c is a code rate. "Sine BOC" and "Cosine BOC" may be identified, depending on the phasing of the subcarrier to the code boundaries. We adopt here nomenclature "BOCs" and "BOCc," respectively.

John Betz, of the MITRE Corporation, introduced the concept of BOC in 1999. Two papers by him, cited in the Additional Resources section near the end of this article, discuss the BOC modulation in greater detail.

Figure 1 illustrates BOCs($2f, f$) where a "square sine" having a frequency twice the code rate is identified. A chip width $T_c = 1/f_c$ and a sub-chip width $T_s = 1/(2f_c)$ may be defined here.

As a consequence of the subcarrier modulation, the spectrum of this new BOC signal is split into two sidebands located above and below the nominal carrier frequency. Although the CDMA principle still applies, the BOC design now admits an element of frequency division multiple access (FDMA). This manifests itself in the multiple sharing of heritage PSK and BOC signals of different subcarrier rates, many of which are sharing the same carrier frequency. (A clear summary of all adopted modulations and processes is given in an article in the

Inside

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September/October 2007 issue of *Inside GNSS*, “The MBOC Modulation.”)

BOC offers some advantages compared to PSK modulation as used by the present-generation GPS. However, a significant problem appears in its practical reception, as attested by many engineering papers and recent practical tests. See for example the papers by P. D. Blunt et alia and A. Simsky et alia listed in Additional Resources.

Essentially, the problem arises from the multi-peaked correlation function characteristic of BOC and the potential for a receiver encountering “false lock” or “false node tracking” on a secondary rather than the primary peak. In this article, we will present a new receiver principle that we believe overcomes this problem in a radical manner. Simulations and early practical tests have provided substantial corroboration that the new solution works.

We will explain here in much greater detail — and offer a more system-

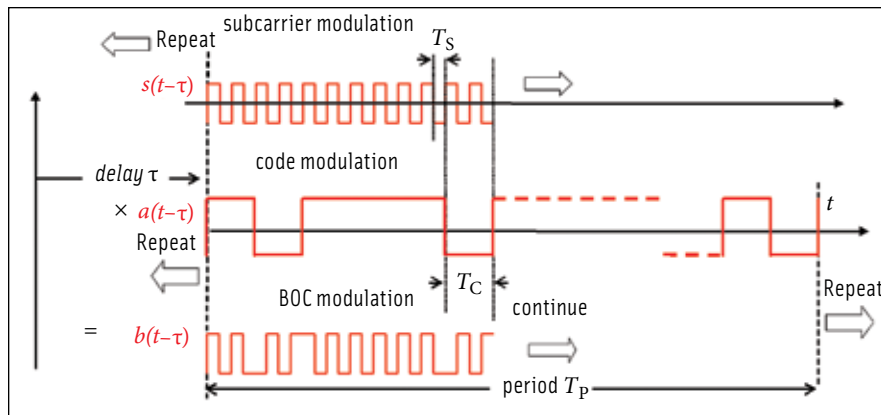


FIGURE 1 Schematic construction of BOCs(2f, f) modulation where $2f = f_s$ and $f = f_c$

atic development — than the succinct account published in the article by M.S. Hodgart and P. D. Blunt cited in Additional Resources.

BOC: A Mathematical Description

The BOC input into any receiver can be described mathematically as in **Equation 1**

$$u(t) = A \times \cos(\omega_0 t + \phi) \times b(t - \tau) \times d \quad 1$$

where A is an amplitude, ω_0 is an intermediate frequency, ϕ is a phase shift on the carrier (which is generally time-varying from Doppler shift), and $b(\cdot)$ is the BOC modulation. Delay τ is the key parameter measured by the receiver (and is also time varying). Parameter $d \in \{-1, +1\}$ denotes either data or an arbitrary

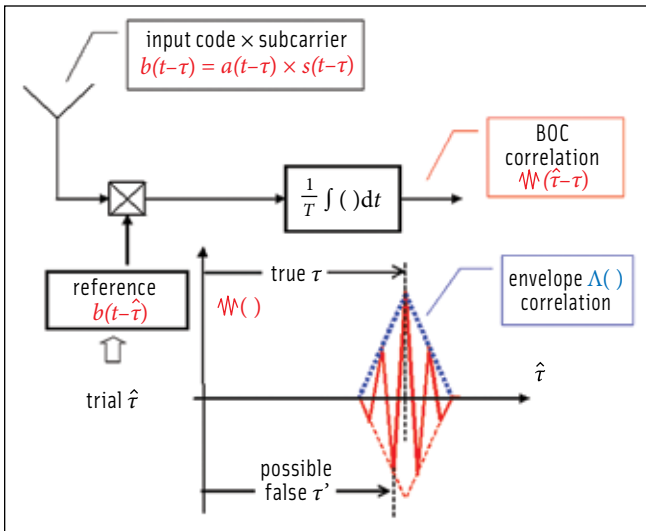


FIGURE 2 Standard cross correlation for BOCs(2f, f)

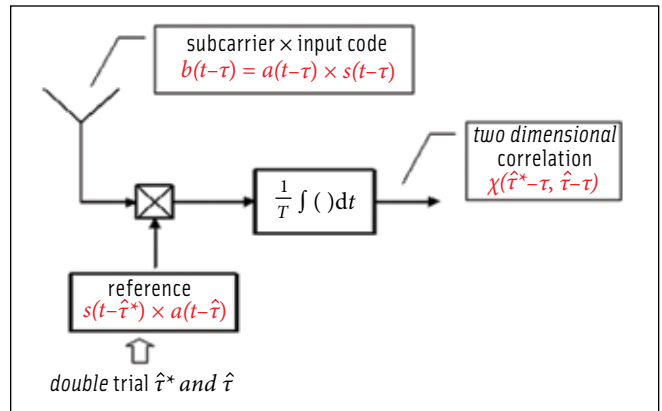


FIGURE 3 Basic principle of a double estimator

bitrary sign value. In Equation 1, the time dependence between phase ϕ and delay τ is left implicit. The actual modulation may be written as in Equation 2,

$$b(t-\tau) = s(t-\tau) \times a(t-\tau) \quad 2$$

which expresses explicitly the product of the code $a(\)$ with periodicity T_p and subcarrier $s(\)$ with periodicity $2T_s$. Naturally the time delay is the same in the two factors.

The presence of additive noise and of many other simultaneous transmissions using different codes is ignored in this simplified representation, which also ignores secondary codes, the concept of “interplexing,” and “AltBOC” of the European proposals.

The fundamental principle of the heritage PSK GNSS receiver systems is to cross-correlate each input signal with a matching reference code and then look for a peak in the resulting Λ -function by effectively varying a trial delay $\hat{\tau}$.

Applying the same principle of cross-correlation on BOC, however, creates a standard multi-peaked function $W(\)$ and the well-known difficulty created by the secondary peaks onto which a correlating receiver (using a discriminator from early and late gates with feedback through a loop) may easily — but incorrectly — lock.

Figure 2 is a schematic representation of the problem in the theoretical case of infinite input receiver bandwidth, and ignoring the matter of carrier demodulation. In addressing the correlation

function and false-node tracking, we should note that negative peaks are just as much a problem as positive ones.

VE-VL or “Bump Jumping”

There is only one previously known fix to the problem of BOC reception that preserves signal-to-noise optimality. It has been implemented in some practical receiver designs and adopts a commonsense approach of so-called “bump-jumping” (B-J). The idea is that additional very-early (VE) and very-late (VL) gates monitor the amplitude of adjacent peaks in $W(\)$. (See the Additional Resources citation of the article by P. Fine and W. Wilson for a useful discussion of this technique.) If a comparison with amplitude on the prompt gate (P) indicates a higher amplitude on either VE or VL, then a condition of false lock is judged to exist and the receiver must make the appropriate jump of either $+T_s$ or $-T_s$, hopefully in the direction of the correct peak.

This method is open to the objection that the receiver is essentially “blind.” It must be in a false lock condition before it knows that it is in this condition. Further, it can only move one sub-chip step at a time, and evaluation of relative amplitudes takes time.

More practical difficulties, which naive computer simulations will fail to replicate, are the effects of front-end filtering, multipath, and, above all, group delay distortion from whatever cause. All of these effects tend to degrade the essential requirement that the amplitude

of the nearest secondary peaks should be significantly less than the amplitude of the main peak. Otherwise, in the unavoidable presence of additive noise causing random fluctuations in the relative amplitudes of different peaks, a mis-correction is a real possibility.

Actual failures of the VE-VL principle have been recorded with what is supposed to be the “easiest” variant, BOCs(1,1). Other more subtle difficulties may become manifest with higher rate ratios of BOC modulations.

New Proposal

Our proposed system does not generate the usual $W(\)$ function, because it envisages the multiplicative components in the correlating waveform as two independent entities.

Figure 3 shows that, with our proposed approach, the reference cross-correlating function is still the product of a matching code function and a subcarrier, but now independent trial delays $\hat{\tau}$ and $\hat{\tau}^*$ are assigned to the code and subcarrier components, respectively.

The resulting correlation $\chi(\)$ is a two-dimensional function of these two different trial values. In the $\hat{\tau}$ dimension, a single peak (alternate positive and negative) is centered on $\hat{\tau} = \tau$. In the $\hat{\tau}^*$ dimension, the multi-valued peaks (positive and negative) are located at $\hat{\tau}^* = \tau + nT_s$, where n is an integer.

Figure 4 depicts the familiar $W(\)$ function alongside the new $\chi(\)$ function. The former is now seen as a one-dimensional cut across the latter in the special case where $\hat{\tau}^* = \hat{\tau}$. An infinite front-end bandwidth is assumed in these computer-generated plots.

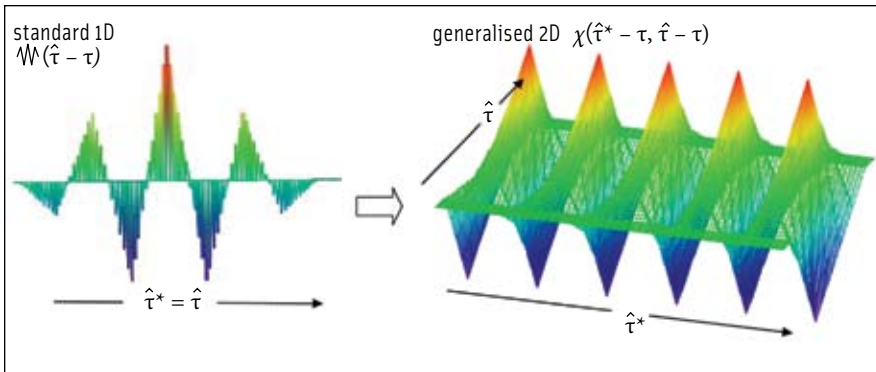


FIGURE 4 Old one-dimensional correlation generalizes to new two-dimensional correlation for BOCs(2f, f)

Figure 5 shows that in the $\hat{\tau}$ dimension for $\hat{\tau}^* = 0$ we are still looking at the familiar Λ -correlation associated with heritage PSK. Its width is the same $\pm T_C$, as if only code modulation were present.

However, in Figure 6 in the $\hat{\tau}^*$ dimension for $\hat{\tau} = 0$, a continuous function of periodicity $2T_s$, now appears, as if only a subcarrier modulation were present. These particular plots are for BOCs(2f, f).

It may be shown that BOCc(2f, f) has the same general characteristic.

2D Correlation Function?

Acquisition in a receiver now has quite a different objective. There need only be a search for the *nearest* peak (positive or negative) of the $\chi(\cdot)$ function, from whatever are the identical initial trial values to $\hat{\tau}^*$ and $\hat{\tau}$. While always subject to jitter from additive noise (and interference), a

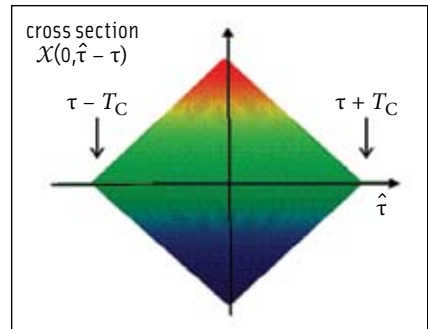


FIGURE 5 Projection of the new correlation for BOCs(2f, f)

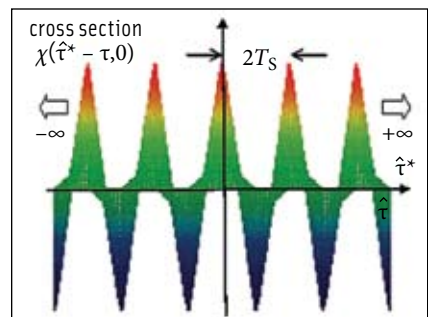


FIGURE 6 Projection of the new correlation for BOCs(2f, f)

Figure 8 shows the characteristic features of a practical system. A BOC-modulated signal input feeds a right-hand circularly polarized antenna and passes into a pre-amplifier that filters the received signal and incorporates a low noise amplifier (LNA) to amplify the received signal.

The LNA effectively sets the receiver's noise figure, normally around 2 dB, and provides about 30 dB gain. The pre-amplifier feeds the filtered, amplified signal to a down-converter for a first stage down-conversion of the signal to a suitable intermediate frequency (IF). The signal is down-converted in multiple stages and filtered to eliminate unwanted image signals.

The down-converter feeds an analog-to-digital converter (ADC). This can quantize the signal to one, two, or more bits. Typically, if the ADC uses multi-bit quantization, the receiver incorporates an automatic gain control (AGC) circuit to maintain proper distribution of the signal across the quantization levels. A reference oscillator provides a clock signal $c(t)$. From the ADC a digital signal $u(t)$ goes to the double estimator of the delay τ between transmission and reception of the received signal.

The receiver includes a correlator stage and a processing stage. In hardware the correlator stage comprises either an application specific integrated circuit (ASIC) or a field programmable gate array (FPGA). The processing stage can be a microprocessor that outputs a delay estimate.

Figure 9 provides a more detailed functional description. It shows the simplest possible coherent system for deriving and processing the error signals, that is, CELP (coherent early-late processing). We should emphasize that a triple-loop implementation will support all the other usual choices of coherent and non-coherent gate processing and discriminator principles, for example NELP (non-coherent early-late processing).

The correlator elements are contained within subsections of **Figure 9** identified by the dotted borders. The remainder is the processing stage. Colors help to identify the underlying processes. The *signal flow* is in red, *reference and clock signals* are in blue, *feedback and processed error signals* are in green, while the *final signal processing* is in gold.

The Concept in Operation

The input signal $u(t)$ has been described according to Equation 1. A clock or reference $c(t)$ is also needed. In the following mathematics, we maintain the convention that every waveform is analog and not quantized in amplitude and time (as it will be in practice).

In the correlator stage, a carrier digital controlled oscillator (DCO) synchronizes to the clock signal $c(t)$ and generates reference signals at the IF ω_0 with trial phase $\hat{\phi}$ represented as in **Equation 6**.

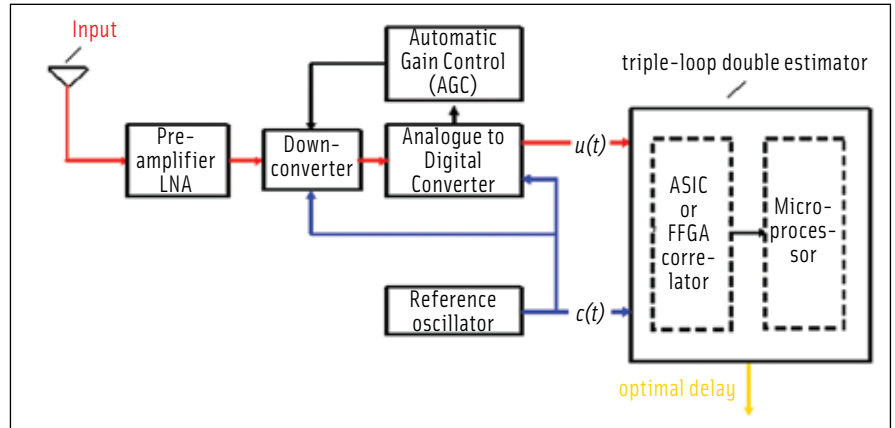


FIGURE 8 Practical structure of input to and output from the triple-loop double-estimator

$$\begin{aligned} r_I(t) &= +\cos(\omega_0 t + \hat{\phi}) \\ r_Q(t) &= -\sin(\omega_0 t + \hat{\phi}) \end{aligned} \quad 6$$

After mixing the input signal, using multipliers, I and Q (in phase and quadrature) signals are derived (neglecting additive noise and other BOC signals simultaneously present) as in **Equation 7**.

$$\begin{aligned} v_I(t) &= A \times \cos(\phi - \hat{\phi}) \times s(t - \tau^*) \times a(t - \tau) \times d \\ v_Q(t) &= A \times \sin(\phi - \hat{\phi}) \times s(t - \tau^*) \times a(t - \tau) \times d \end{aligned} \quad 7$$

A subcarrier DCO uses the clock signal to generate Prompt (P), Early (E), and Late (L) gate subcarrier reference signals $s(t - \hat{\tau}^*)$, $s(t - \hat{\tau}^* + T_{DS}/2)$ and $s(t - \hat{\tau}^* - T_{DS}/2)$ respectively, where $\hat{\tau}^*$ is a trial subcarrier delay and T_{DS} is the total separation between the E and L gates.

Here we maintain the convention that $T_{DS} = T_s$. Similarly, a code DCO uses the clock signal to generate P, E, and L gate code reference signals $a(t - \hat{\tau})$, $s(t - \hat{\tau}^* + T_{DC}/2)$ and $s(t - \hat{\tau}^* - T_{DC}/2)$, respectively, where $\hat{\tau}$ is a trial code delay and T_{DC} is the total separation between E and L gates. The separation T_{DC} can be selected in the range $T_s \leq T_{DC} \leq T_c$.

The correlator block continues by multiplying the I and Q signals with appropriate combinations of the P, E, and L gate subcarrier reference signals and the P, E, and L gate code reference signals in order to generate six demodulated signals $v_{III}(t)$, $v_{IEI}(t)$, $v_{ILI}(t)$, $v_{IIE}(t)$, $v_{IIL}(t)$, and $v_{QII}(t)$ as in **Equations 8**.

$$\begin{aligned} v_{III}(t) &= v_I(t) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau}) \\ v_{IEI}(t) &= v_I(t) \times s(t - \hat{\tau}^* + T_{DS}/2) \times a(t - \hat{\tau}) \\ v_{ILI}(t) &= v_I(t) \times s(t - \hat{\tau}^* - T_{DS}/2) \times a(t - \hat{\tau}) \\ v_{IIE}(t) &= v_I(t) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau} + T_{DC}/2) \\ v_{IIL}(t) &= v_I(t) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau} - T_{DC}/2) \\ v_{QII}(t) &= v_Q(t) \times s(t - \hat{\tau}^*) \times a(t - \hat{\tau}) \end{aligned} \quad 8$$

These demodulated signals are derived by successive use of multipliers. They are then integrated to various correlations. The integrators run over a fixed time T_i which can be the same as the code period T_p or an integer multiple of this code period.

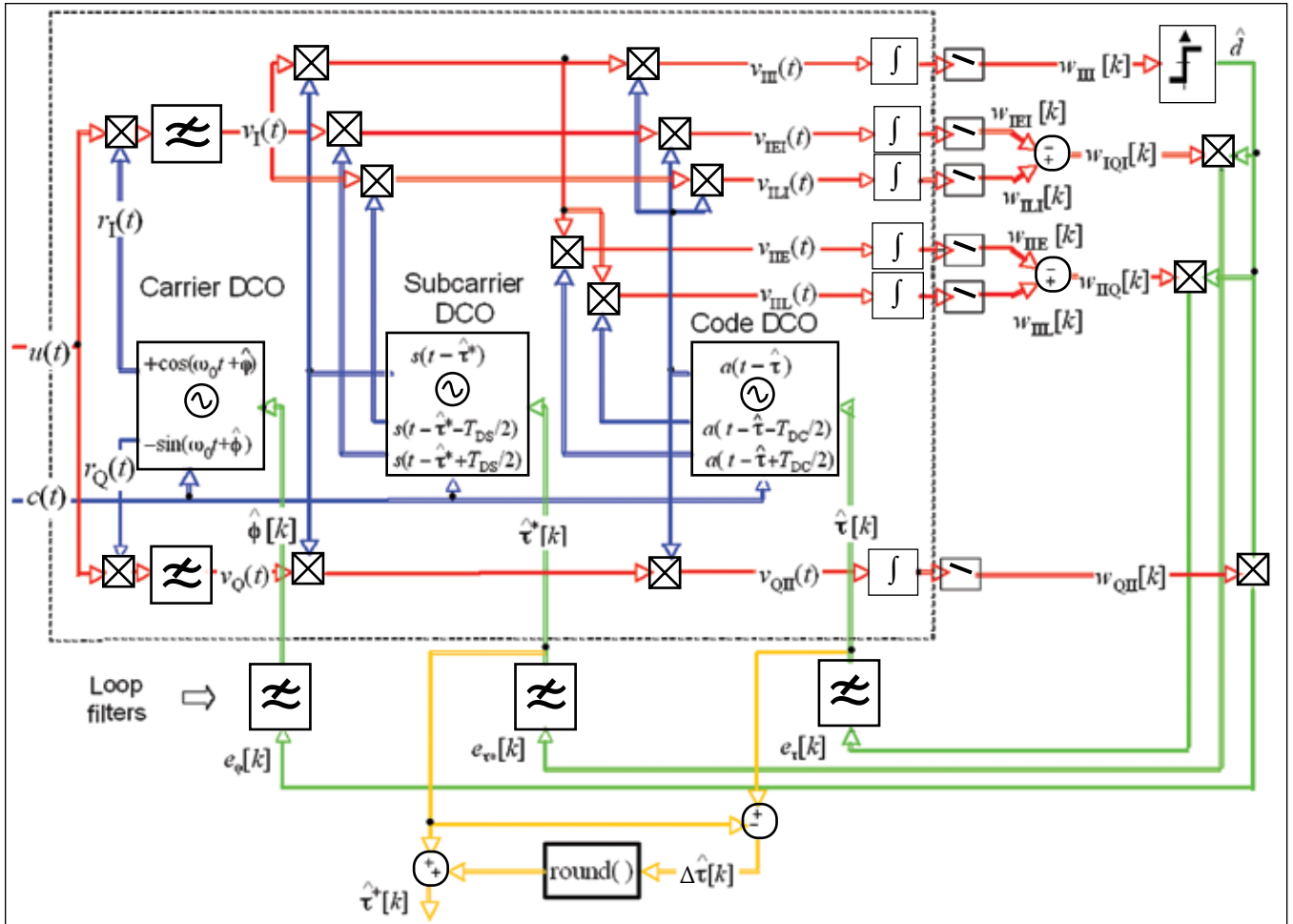


FIGURE 9 Schematic structure of a triple-loop double-estimator (a coherent early late processing or CELP implementation) showing signal flow (red), reference and clock signals (blue), feedback and processed error signals (green), and final signal processing (gold).

The outputs of the integrators can be described as a set of six correlations $w_{III}[k]$, $w_{IEI}[k]$, $w_{IIL}[k]$, $w_{IIE}[k]$, $w_{IIL}[k]$, and $w_{QII}[k]$ for an ever-increasing correlation count $k = 1, 2, 3, \dots$. The output of each of the integrators is sampled by the processing stage at the end of each fixed time and then the integrators are reset to zero. (Note: Count “ k ” is provided here for explanatory purposes and need not be specifically recorded in any algorithm.)

The values of the k 'th correlations depend on the difference between the k 'th trial phase $\hat{\phi} = \hat{\phi}[k]$ and the true phase ϕ , the difference between the k 'th trial subcarrier delay $\hat{\tau}^* = \hat{\tau}^*[k]$ and the true delay τ , and the difference between the k 'th trial code delay $\hat{\tau} = \hat{\tau}[k]$ and the true code delay τ . The I subcarrier P gate and code P gate correlation is given precisely in Equation 9 and approximately as in Equation 10.

$$w_{III}[k] = A \times \cos(\phi - \hat{\phi}[k]) \times \chi(\hat{\tau}^*[k] - \tau, \hat{\tau}[k] - \tau) \times d \quad 9$$

$$w_{IIL}[k] \approx A \times \cos(\phi - \hat{\phi}[k]) \times \text{trc}(\hat{\tau}^*[k] - \tau) \times \Lambda(\hat{\tau}[k] - \tau) \times d \quad 10$$

In these equations $\text{trc}()$ is a continuous triangular cosine of periodicity $2T_{DS}$, and $\Lambda()$, as always, is the familiar correlation function of a PSK-modulated signal having the same code rate as the received signal. The acceptability of these approxima-

tions can be appreciated by referring back to Figure 5, where the cross-section view of the two-dimensional function $\chi()$ in the dimension of the trial code delay $\hat{\tau}$ is identical to PSK correlation $\Lambda()$. Correspondingly, Figure 6 shows that $\chi()$ in the dimension of the trial subcarrier delay $\hat{\tau}^*$ is sufficiently similar to a $\text{trc}()$ function.

The other correlations are likewise sufficiently well approximated (with an implicit dependence on k) as in Equations 11.

$$\begin{aligned} w_{IEI}[k] &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau - T_{DS}/2) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{IIL}[k] &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau + T_{DS}/2) \times \Lambda(\hat{\tau} - \tau) \times d \\ w_{IIE}[k] &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau - T_{DC}/2) \times d \\ w_{IIL}[k] &\approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau + T_{DC}/2) \times d \\ w_{QII}[k] &\approx A \times \sin(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \end{aligned} \quad 11$$

The difference between appropriate early and late correlations creates discriminator functions according to Equation 12 and Equation 13.

$$w_{IQI}[k] = w_{ILI}[k] - w_{IEI}[k] \\ \approx A \times \cos(\phi - \hat{\phi}) \times \text{trs}(\hat{\tau}^* - \tau) \times \Lambda(\hat{\tau} - \tau) \times d \quad 12$$

$$w_{IIQ}[k] = w_{IIL}[k] - w_{IIE}[k] \\ \approx A \times \cos(\phi - \hat{\phi}) \times \text{trc}(\hat{\tau}^* - \tau) \times \sqrt{\Lambda}(\hat{\tau} - \tau) \times d \quad 13$$

In these equations $\text{trs}()$ is a *triangular periodic discriminator function* that goes through zero for $\hat{\tau}^* = \tau + nT_s$, and $\sqrt{\Lambda}()$ is a discriminator function derived from early and late differences of the Λ function and goes through zero uniquely for $\hat{\tau}[k] = \tau$.

The four correlations $w_{III}[k]$, $w_{QII}[k]$, $w_{IQI}[k]$ and $w_{IIQ}[k]$ contain the information necessary to drive the three loops in a basic CELP.

As shown here, in the processing stage, there is a limiter to estimate the sign of the I subcarrier P gate and code P gate correlation (which may be either positive or negative). Expressed mathematically, this reads as in **Equation 14**

$$\hat{d} \leftarrow \text{sgn}(w_{III}) \quad 14$$

In this implementation these error signals $e_\phi[k]$, $e_{\tau^*}[k]$ and $e_\tau[k]$ are generated from the correlations in order to steer the trial phase $\hat{\phi}$, trial subcarrier delay $\hat{\tau}^*$, and trial code delay $\hat{\tau}$, respectively, toward the true phase ϕ , true delay τ plus or minus some integer multiple of T_s , and absolute true delay τ , respectively.

Every completed correlation period T the errors may then be computed, notated above as an event by a unit increment in count k . In **Equations 15** the count record $[k]$ is deliberately omitted here, because in the actual algorithm this count does not need to be recorded.

$$e_\phi \leftarrow w_{QII} \times \hat{d} \\ e_{\tau^*} \leftarrow w_{IQI} \times \hat{d} \\ e_\tau \leftarrow w_{IIQ} \times \hat{d} \quad 15$$

The loop filters process the errors in order to increment or decrement the trial phase $\hat{\phi}$, subcarrier trial delay $\hat{\tau}^*$, and code trial delay $\hat{\tau}$ appropriately. These actions can be expressed iteratively as in **Equation 16**

$$e_\phi \leftarrow f_\phi + e_\phi \\ \hat{\phi} \leftarrow \hat{\phi} + a_1 f_\phi + a_2 e_\phi \\ \hat{\tau}^* \leftarrow \hat{\tau}^* + a_{\tau^*} e_{\tau^*} \\ \hat{\tau} \leftarrow \hat{\tau} + a_\tau e_\tau \quad 16$$

In this CELP implementation the PLL is second order and controlled by two gain constants a_1 and a_2 ; the SLL is first order, controlled by a gain constant a_{τ^*} ; and the DLL is also first order, controlled by a gain constant a_τ . With increasing count and in the realistic presence of noise these errors go to zero on average, i.e. $e_\phi[k] \rightarrow 0$, $e_{\tau^*}[k] \rightarrow 0$ and $e_\tau[k] \rightarrow 0$.

Although the SLL and the DLL each require the other to have converged, the values to their two emerging estimates

are independent of each other, the first being derived from the timing of the subcarrier component and the second from the timing of the code component.

In a final stage, the two estimates can then be linked, because the difference between them, after rounding, should be an integer multiple of the sub-chip width T_s , for both loops being locked (converged). Therefore, on every correlation the two independent estimates are combined into a single estimate according to Equation 4, where the ambiguity in the higher accuracy $\hat{\tau}^*$ is automatically corrected by the unambiguous lower accuracy $\hat{\tau}$. Provided the time jitter is not excessive, so that constraint of Equation 5 is observed, this calculation will automatically find the needed integer correction.

Generalizations

More sophisticated strategies and developments have been developed, staying within the basic concept, such as the following:

1. Calculation Equation 4 can be performed implicitly. There need only be the two estimates, where the best $\hat{\tau}^* = \hat{\tau}^*$ estimate is automatically “booted” up or down by integer multiples of T_s , from within the SLL, by continuous comparison with the rounded difference from the $\hat{\tau}$ code estimate.
2. At the cost of requiring a total of eight rather than four correlations, an “incoherent DLL+SLL” may be realized in which a frequency-locked loop FLL replaces the PLL.
3. The wide variety of different discriminator designs known to the standard two-loop PSK correlation receivers may be adopted — including non-coherent early-late processing.
4. The standard technique known as “carrier aiding” may be incorporated.
5. The receiver concept readily generalizes to deal with the European AltBOC concept.
6. Adaptive gate width in the DLL may be adopted to implement faster loop acquisition in low C/N_0 conditions.

Evaluation and Comparison with VE-VL Receiver

The inherent property of BOC is that an estimate of delay from the subcarrier component alone may be “out” by an arbitrary integer number of sub-chips. This is our SLL estimate. However, this ambiguity is of no consequence for us because we *also* have the independent DLL estimate. And the key difference with our method, compared to bump-jumping, is that once the loops are in lock then evaluation of the necessary integer correction to the SLL estimate is “hard directed” and instantaneous.

Our method requires no doubtful dependence on the monitoring of the amplitudes of secondary and main peaks. In any case, these different amplitudes no longer exist. Further, the existence of two independent estimates offers a variety of safety checks, because of the independence of the two estimates. In particular, what was otherwise shaping up to be a major problem with BOC — group delay distortion — can be expected to be readily and automatically “calibrated out” from longer term averaging and comparison of the two estimates.

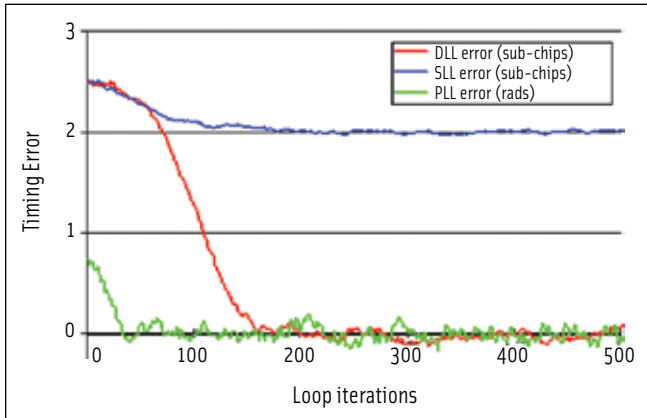


FIGURE 10 Acquisition of two (DLL and SLL) estimates and the carrier phase (PLL)

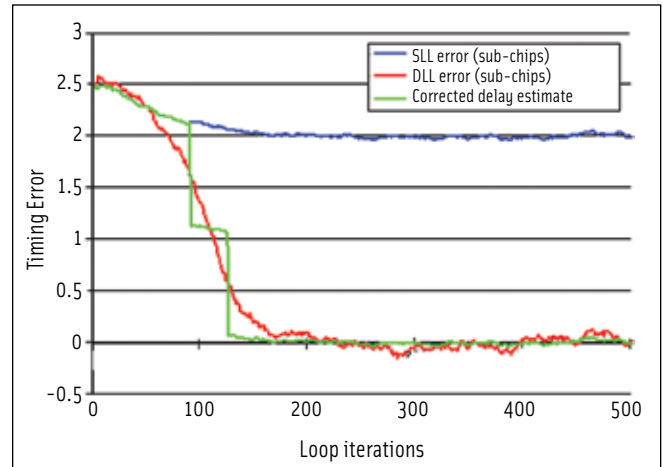


FIGURE 11 Acquisition of two estimates and corrected estimate

Simulations

An example computer simulation of the double estimating concept is shown in **Figure 10** for a BOC(2f, f) signal. The MATHCAD simulation assumes equal DLL and SLL bandwidths (1 Hz) and $C/N_0 = 30$ dBHz. The initial delay offset was set at 2.5 sub-chips and an initial phase error to the carrier component of $\pi/4$. The numerical count (horizontal axis) is of completed correlations.

Under loop operation the DLL estimate (red) is seen to provide unambiguous tracking. The timing jitter is the same as one would get for an equivalent receiver tracking PSK. disturbance. The SLL delay estimate (blue) delivers the lower timing jitter associated with BOC; however, this estimate is ambiguous, locking to the nearest subcarrier correlating peak, which in this case happened to be 2 sub-chips away from the truth.

Figure 11 provides an example of acquisition and tracking, now showing a corrected estimate (in green) according to Equation 4. The figure shows distinctly that this corrected value has the lower jitter of the SLL estimate and the unambiguous location of the PLL estimate.

A potential problem for VE-VL bump-jumping with BOC is *group delay distortion* from whatever cause. As is well known from the physics, the effect of such a distortion on the standard correlation function $\mathcal{W}(\cdot)$ is a shift of the alternating peaks of the subcarrier component relative to the overall Λ envelope. The inevitable effect for the

VE-VL principle is to reduce the amplitude margin between secondary peaks and the main peak, and increase the risk of false lock.

The condition of group delay distortion should not however be a problem for a double estimating receiver. The effect is readily reproduced as seen in **Figure 12** and is revealed by a corresponding offset in the steady state differences, which is not an integer multiple of T_s . Because its two estimates are independent the double estimator has the potential to estimate this difference by longer term averaging. This means that one could design an automatic calibration in the signal processing in order to compensate for this effect.

Another key performance measure of particular interest is that of the multipath. The simplest method of evaluating the multipath error performance is to consider the effect of a single interfering multipath signal with various relative time delays. This provides only a worst-case analysis of error due to multipath but does provide an adequate performance measure with which we can compare BOC tracking schemes.

Figure 13 shows the multipath error envelopes of a conventional BOC receiver and the dual estimator for a BOC(2,1) signal. The dual estimator error envelope is computed by analyzing the error of the corrected SLL delay estimate with multipath interference.

We can see the relative performance of each scheme by computing the running average error across the dataset,

as shown in **Figure 14**. The pattern of the dual estimator multipath envelope broadly follows that of the conventional receiver but does show a small improvement (8.2 percent) across the whole dataset.

Experimental test

Surrey Satellite Technology was responsible for construction and control of the first test satellite GIOVE-A (Galileo In-Orbit Validation Element) for the Galileo project on behalf of the European Space Agency (ESA). Subsequently, with the cooperation of ESA, some of the signals were monitored at the University of Surrey.

After testing its feasibility on simulated bench source signals, the GIOVE A BOC(1,1) signal-in-space transmission was monitored, with a research-developed single-chip receiver with properties as described in **Table 1**.

The signal was successfully acquired on June 26, 2006, at 19.57 GMT with an estimated receiver carrier-to-noise density ratio of 45 dBHz. **Figure 15** shows the corresponding I/Q plot taken from GIOVE-A tracking. We have demonstrated, therefore, that the principle of double estimation works in practice, for one particular BOC modulation.

Development

The relative simplicity of a GNSS receiver architecture based on the double estimating concept provides an attractive choice for the designer. In particular a double estimating receiver is com-

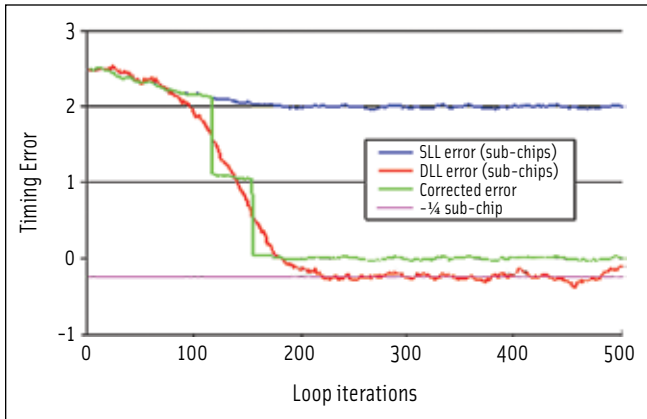


FIGURE 12 Showing effect of delay distortion on the sub carrier offset by $\frac{1}{4}$ sub-chip

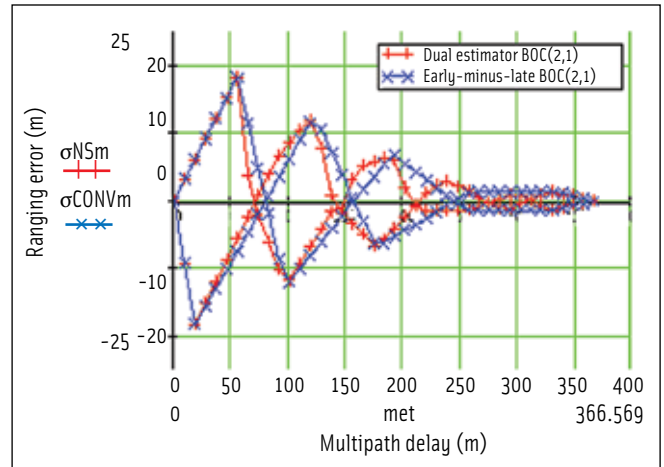


FIGURE 13 Multipath error envelope of a conventional and dual estimating BOC receiver, BOC(2,1), $T_{DC} = T_{DS} = T_S$

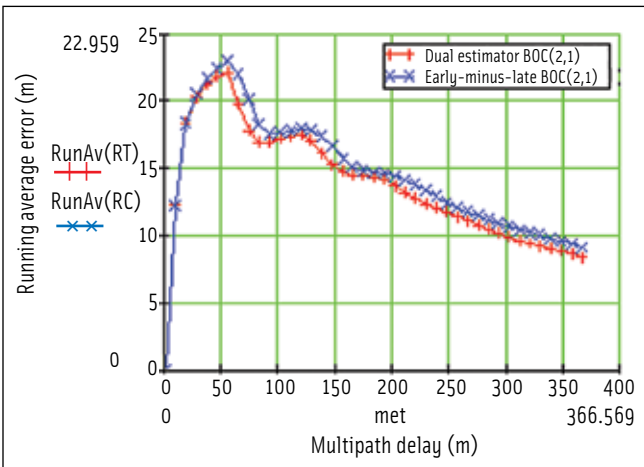


FIGURE 14 Running average multipath error of a conventional (blue line) and dual-estimating BOC receiver $T_{DC} = T_{DS} = T_S$ for BOC(2,1),

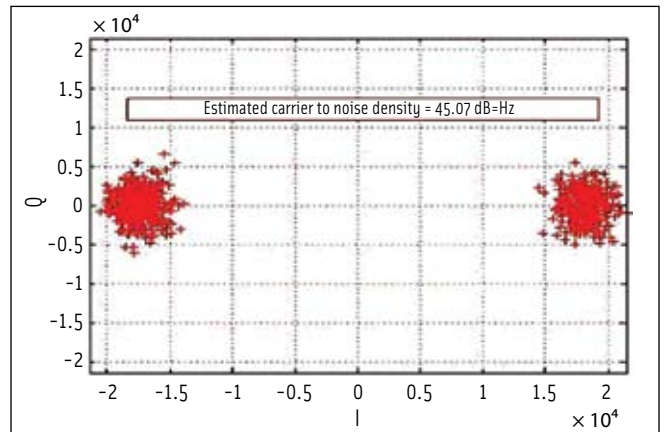


FIGURE 15 I/Q plot GIOVE-A in PLL mode

patible with the leading unambiguous BOC search technique named by its originator as “replica code design” (for a further discussion of this technique, see the paper by P. Ward in Additional Resources.)

Adoption of this search technique will deliver a common start value to the subcarrier delay estimate $\hat{\tau}^*$ and the code estimate $\hat{\tau}$ within the range $\pm T_C$ i.e. initially $\hat{\tau}^* = \hat{\tau}$. A double estimating receiver requires little more than uncoupling of these initial estimates under command, allowing the two independent tracking estimates to emerge as expected in Equation 3, and requiring then a rounded integer correction according to Equation 4. All other proposed BOC tracking techniques will require additional hardware resources to become compatible with this excellent search technique.

The hardware required for the dual estimator and the leading BOC tracking techniques is compared in Table 2 for correlator designs requiring fully *incoherent* operation.

The double estimator and the bump-jumping (VE-VL) algorithm both make efficient use of a receiver’s hardware resource. Admittedly we use two additional multipliers and the additional local oscillator when compared to that

	BOC (1,1) RF receiver
RF Front End	A double super-heterodyne receiver for the GNSS L1/E1 band
Sampling Frequency	16.367 MHz
IF	4.188MHz
Correlator	FPGA
Processor	Leon3 Sparc V8 (FPGA based)
Signals Received	Galileo L1-B/C – BOC(1,1)

TABLE 1. Tested receiver characteristics

Receiver type	Multipliers	Integrators	Local oscillators	Low pass filters
Single-sideband	2×Carrier, 4×Code	4	1×Carrier, 1×Code	2
Multiple Gate Discriminator (N=4)	2×Carrier, 18×Code	18	1×Carrier, 1×Code	0
Bump Jumping	2×Carrier, 10×Code	10	1×Carrier, 1×Code	0
Dual Estimator	2×Carrier, 4×Subcarrier 8×Code	8	1×Carrier, 1×Subcarrier, 1×Code	0

TABLE 2. Hardware requirements of BOC tracking techniques

algorithm. However, the additional multipliers are one-bit, and therefore the limiting factor in designs will be the number of storage elements used (integrators). A double estimator receiver uses two less integrators per channel than the VE-VL algorithm. Examples of hardware resource utilization for a prototype BOC receiver are given in the paper by P. D. Blunt.

Simulations indicate that, in principle, the receiver should be able to cope with the European BOC(15, 2.5) signal on which difficulties have been reported using the bump-jumping technique. Development has begun to demonstrate this in practice.

Conclusion

The double estimator has been demonstrated to work through extensive simulation, with bench tests on a BOC(1,1) signal generated by an SSTL-built Galileo signal generator, and finally with live signals from the GIOVE-A satellite.

Many experimental tests on these real BOC signals confirm that convergence of a double-estimator triple-loop receiver is smooth and stable. Performance in noise and multipath seems satisfactory. The design is believed to be inherently tolerant and adaptive to group delay distortion.

Simulations indicate that, in principle, the receiver should be able to cope with the European BOC(15, 2.5) signal on which difficulties have been reported using the bump-jumping technique. Development has begun to demonstrate this in practice.

A patent application was initially registered to the University of Surrey in the name of the inventors (Hodgart and Blunt) Reg. no GB0624516.1. An international patent application was subsequently filed and has been recently published.

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Manufacturers

The receiver developed using the BOC-tracking technique described in this article used the NJ1006A RFIC from **NemeriX**, Manno, Switzerland. The

test receiver developed using the BOC-tracking technique described in this article used the NJ1006A RFIC from **NemeriX**, Manno, Switzerland. The correlators were implemented on a Spartan 3 FPGA from **Xilinx**, San Jose, California, USA. The control of the receiver's tracking loops was achieved using the Leon SPARC V8 processor from **Gaisler Research**, Gotenborg, Sweden.

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He holds a B.Sc. from Lancaster University and a Ph.D. from the University of Surrey. 